UM10059

ISP1109 PC Eval Kit

Rev. 01 — 2 November 2005

User manual

Semiconductors

Document information

Info	Content
Keywords	isp1109; universal serial bus, usb, transceiver, spi, carkit, i2c
Abstract	The ISP1109 evaluation (eval) board is designed to verify the functions of the ISP1109 chip.

PHILIPS

Revision history

Rev	Date	Description
01	20051102	First release.

Contact information

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For sales office addresses, please send an email to: **sales.addresses@www.semiconductors.philips.com**

1. Introduction

The ISP1109 is a Universal Serial Bus (USB) transceiver that supports *CEA-936-A, Mini-USB Analog Carkit Interface* specification.

The ISP1109 evaluation (eval) board is designed to verify the functions of the ISP1109 chip. The board consists of the ISP1109 chip, USB mini-AB connector, Serial Parallel Interface (SPI), Inter-IC bus (I^2C-bus) serial interface, analog audio interface, and USB controller interface. The operation mode, and status and control registers of the ISP1109 can be configured through the SPI bus or I^2C-bus interface.

The ISP1109 board can function in two modes: parallel and ISA. The default setting of the board is parallel. In parallel mode, the ISP1109 board is connected to the parallel port of a Personal Computer (PC). In ISA mode, the ISP1109 board is connected to the ISA port of the PC.

The evaluation is performed using a DOS test program on the PC. To fully verify the USB functions of the ISP1109, a USB controller interface connector is required to connect the ISP1109 board to the USB controller.
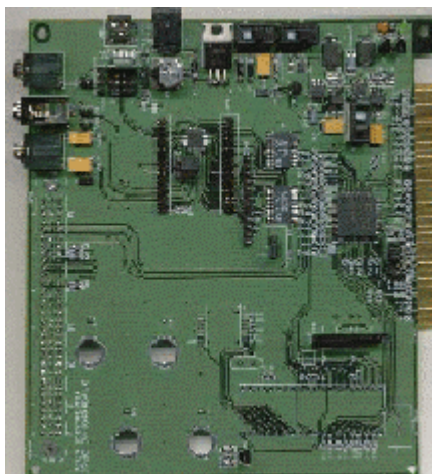

Fig 1.   ISP1109 eval board

2. System requirements

For the development PC:
- PC with ISA slot or parallel port and Microsoft DOS 6.x
- ISP1109 eval board
- Cable and power supply for parallel port mode connection.

For the firmware development:
- x86 CPU platform: Borland Turbo C++ 3.0 or later
- ISP1109 eval diskette.

For the USB test:
- PC with USB motherboard or add-on card
- USB controller.

For the audio test:
- 32 Ω stereo headphones with 3.5 mm stereo plug

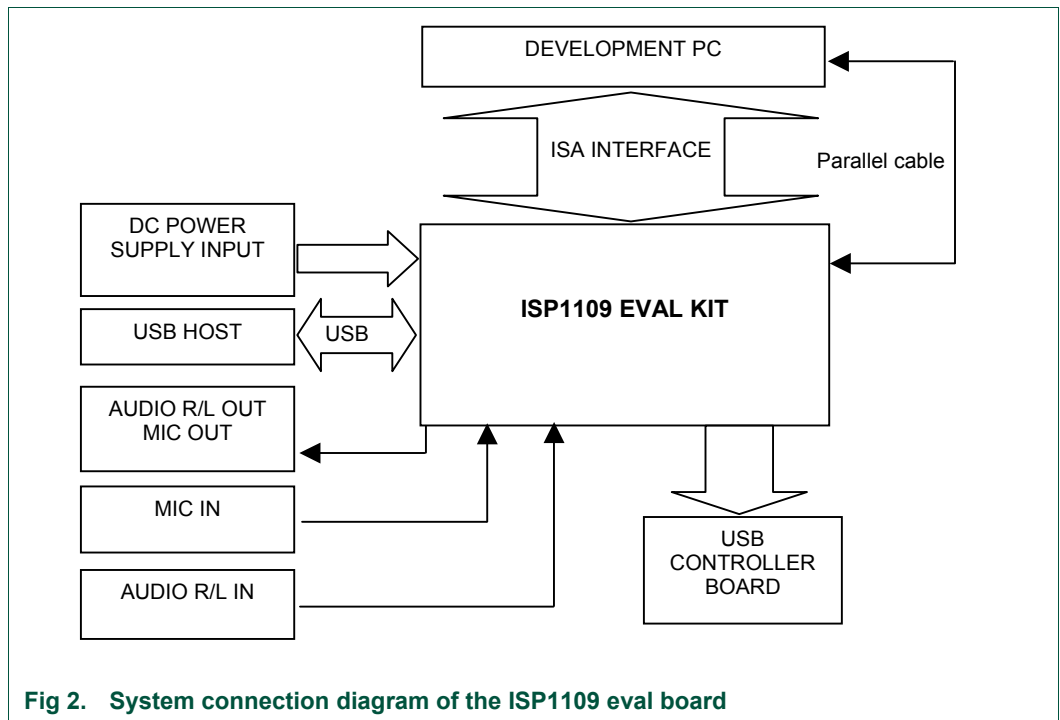• Stereo audio source for 32 Ω stereo headphones.

3. Connection diagram

Fig 2.   System connection diagram of the ISP1109 eval board

4. Configuration and settings

Table 1:   S5 power selection

Board power supply		Self-powered (default)	Bus-powered
Switch on		1	3

Table 2:   S6 power selection

ISP1109 core power supply	Self-powered (default)	Bus-powered
Switch on	3	1

Table 3:   S7 power selection

ISP1109 I/O power supply	$V_{CC(I/O)}$ = 1.8 V	$V_{CC(I/O)}$ = 3.3 V (default)
Switch on	1	3
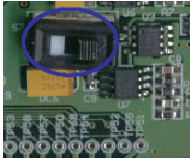
Table 4:   S3 power selection

Microprocessor power supply	5 V (default)	3.3 V
Switch on	V_{CC}	$V_{CC(3V3)}$
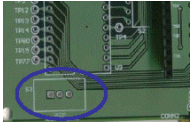
Table 5:   JP1

Isolate level shift	Transmit	Isolate (default)
Short pins	1–OE	$V_{CC(3V3)}$–OE
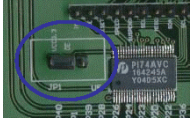
Table 6:   JP10

IRQ number	IRQ3	IRQ4	IRQ5	IRQ6	IRQ7
Short pins	9–10	7–8	5–6	3–4	1–2
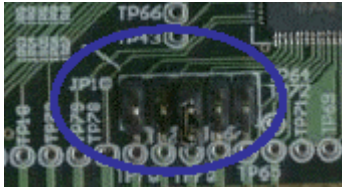
Table 7:   JP3

DP mode switch		USB (default)	Audio	UART	External pull-up
Short pins		1–2	3–4	5–6	7–8
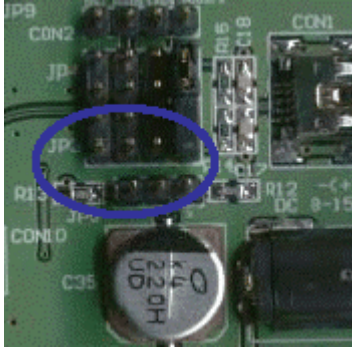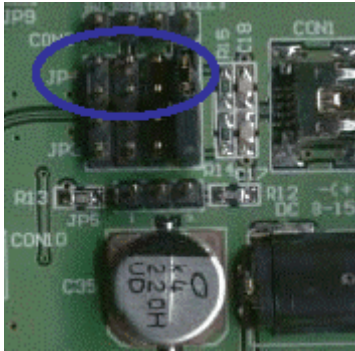
Table 8:   JP4

DM mode switch		USB (default)	Audio	UART	External pull-up
Short pins		1–2	3–4	5–6	7–8

5. PC resources assignment

5.1 Parallel mode

In parallel mode, the ISP1109 eval board occupies three I/O locations. The base address is the address of LPT1. Table 9: provides the I/O mapping for parallel mode.

Table 9:   I/O mapping

Offset	Usage		
0	Data register; write only		
	Data write: bit mapping		
	Bit number	**I/O name**	**Description**
	0	CS	**0**—Drive the CS pin LOW **1**—Drive the CS pin HIGH.
	1	SCL	**0**—Drive the SCL pin HIGH **1**—Drive the SCL pin LOW.
	2	SEL	**0**—Drive the SEL pin LOW **1**—Drive the SEL pin HIGH.

Offset	Usage			
	3	SUSPEND	**0—**Drive the SUSPEND pin LOW **1—**Drive the SUSPEND pin HIGH.	
	4	SPEED	**0—**Drive the SPEED pin LOW **1—**Drive the SPEED pin HIGH.	
	5	RESET	**0—**Drive the RESET pin LOW **1—**Drive the RESET pin HIGH.	
1	Status register; read only			
	Write: bit mapping			
	Bit number	**I/O name**	**Description**	
	5	SDA	**0—**SDA pin outputs LOW **1—**SDA pin outputs HIGH.	
	6	MISO	**0—**MISO pin outputs LOW **1—**MISO pin outputs HIGH.	
	7	INT	**0—**INT pin outputs HIGH **1—**INT pin outputs LOW.	
2	Control register; write only			
	Write: bit mapping			
	Bit number	**I/O name**	**Description**	
	0	SDA	**0—**Drive the SDA pin HIGH **1—**Drive the SDA pin LOW.	

5.2 ISA mode

In ISA mode, the ISP1109 eval board occupies eight I/O locations. The base address is 368h.

Table 10: I/O mapping

Offset	Usage		
0	Data register for SPI mode; data: read/write only.		
2	I/O control register		
	Data write: bit mapping		
	Bit number	**I/O name**	**Description**
	0	SEL	**0—**Drive the SEL pin LOW, SPI mode **1—**Drive the SEL pin HIGH; I^2C-bus mode.
	1	RDWR	**0—**Drive the RDWR pin HIGH, MOSI_SDA output **1—**Drive the RDWR pin LOW; MOSI_SDA input.
	2	SPEED	**0—**Drive the SPEED pin LOW **1—**Drive the SPEED pin HIGH.
	3	SUSPEND	**0—**Drive the SUSPEND pin LOW **1—** Drive the SUSPEND pin HIGH.

Offset	Usage		
	4	RESET	**0**—Drive the RESET pin LOW **1**—Drive the RESET pin HIGH.
	5	CLK_SCL	If bit 0 is logic 1 (I^2C-bus mode): **0**—Drive the CLK_SCL pin LOW **1**—Drive the CLK_SCL pin HIGH. If bit 0 is logic 0 (SPI mode), this bit is reserved.
	6	MOSI_SDA	If bit 0 is logic 1 (I^2C-bus mode) and bit 1 is logic 1: **0**—Drive the MOSI_SDA pin LOW **1**—Drive the MOSI_SDA pin HIGH. If bit 0 is logic 0 (SPI mode), this bit is reserved.
	7	CS_ADR	If bit 0 is logic 1 (I^2C-bus mode): **0**—Drive the CS_ADR pin LOW **1**—Drive the CS_ADR pin HIGH. If bit 0 is logic 0 (SPI mode), this bit is reserved.
	Data read: bit mapping		
	Bit number	**I/O name**	**Description**
	0	MOSI_SDA	If bit 0 is logic 1 and bit 1 is logic 0: **0**—MOSI_SDA pin outputs LOW **1**—MOSI_SDA pin outputs HIGH. If bit 0 is logic 0, this bit is reserved.
	1	INT_N	**0**—INT_N pin outputs LOW **1**—INT_N pin outputs HIGH.
	2	RXD	**0**—RXD pin outputs LOW **1**—RXD pin outputs HIGH.
	3	ISET	**0**—ISET pin outputs LOW **1**—ISET pin outputs HIGH.
	4 to 7	Reserved	
4	Address register; set register address for the SPI host control (SPI mode); data: write only.		
	Write: bit mapping		
	Bit number	**I/O name**	**Description**
	0 to 4	Register address	**0**—Drive the SEL pin LOW, SPI mode **1**—Drive the SEL pin HIGH; I^2C-bus mode.
	5	RD_WR_EN	**0**—Drive the RDWR pin HIGH, MOSI_SDA output **1**—Drive the RDWR pin LOW; MOSI_SDA input.
	6	Start	**0**—Drive the SPEED pin LOW **1**—Drive the SPEED pin HIGH.
	7	INT_EN	**0**—Do not bypass INT_N to IRQ **1**—Bypass INT_N to IRQ.
5 to 7	Reserved		

6. Installing the software and firmware

There are two software modes available in the kit: test and functional. Test mode is for Integrated Circuit (IC) verification, and functional mode is for application testing.

6.1 Parallel mode

6.1.1 Test mode

The port is connected to the parallel port of the development PC. To perform verification using test mode:

1. Set all switches and jumpers to their default states.

2. Connect the DB25 connector of the parallel cable to the LPT1 port of the development PC.

3. Connect the header connector of the parallel cable to CON4 of the ISP1109 eval board.

4. Run firmware 1109PA.EXE on the development PC under DOS mode.

Fig 3.   Main menu

5. Select access mode as SPI or I^{2}C-bus by pressing the **S**[1] or **I** key, respectively. Default is SPI.

6. Select user mode as test mode by pressing the **T** key.

Fig 4.   Test mode menu

7. Select the appropriate test action.

---

1.   In this document, items that you type or click are indicated in **bold**.

D: Data input — Input data for writing to the register.

A: Address input — Input register address to write data to or read data from.

R: Read register — Read data from the Address register.

W: Write register — Write data to the Address register.

F: CLK SWITCH off — Switch off the ISP1109 internal clock.

N: CLK SWITCH on — Switch on the ISP1109 internal clock.

G: List all registers — Read and display all the registers.

L: Interrupt en_low — Set interrupt EN_LOW to verify whether the interrupt action is correct.

U: Interrupt en_high — Set interrupt EN_HIGH to verify whether the interrupt action is correct.

H: Hard Reset ISP1109 — Reset the ISP1109.

Esc: Exit to Main Menu — Return to the main menu.

6.1.2 Functional mode

The port is connected to the parallel port of the development PC. To perform verification using functional mode:

1. Set JP3 and JP4 based on the selected states. Set all other switches and jumpers to their default states. Plug audio source into the AUDIO_OUT port, headphones into the AUDIO_IN port, and microphone source into the MIC_IN port. Connect the USB controller to CON3.

   - **USB mode**: Short JP3 1–2, JP4 1–2.
   - **Audio mode**: Short JP3 3–4, JP4 3–4.
   - **UART mode**: Short JP3 5–6, JP4 5–6, CON2 2–3.

2. Connect the DB25 connector of the parallel cable to the LPT1 port of the development PC.

3. Connect the header connector of the parallel cable to the CON4 of the ISP1109 eval board.

4. Run firmware 1109PA.EXE on the development PC under DOS mode.

Fig 5.   Main menu

5. Select access mode as SPI or I^{2}C-bus by pressing the **S** or **I** key, respectively. Default is SPI.

6. Select user mode as functional by pressing the **F** key.

Fig 6.   Test menu

7. Select the appropriate functional mode.

P: Pin — USB speed and suspend are controlled by the SPEED and SUSPEND pins.

R: Register — USB speed and suspend are controlled by the SPEED_REG and SUSPEND_REG register bits.

F: Full speed — Set USB speed to full-speed.

L: Low speed — Set USB speed to low-speed.

A: Active — Wake up from the suspend state.

S: Suspend — Go into the USB suspend state.

U: USB_VPVM_U — Connect the USB controller to CON3, and connect USB cable from CON1 to USB host. The board system will work as a USB peripheral.

V: USB_VPVM_B — Connect the USB controller to CON3, and connect USB cable from CON1 to USB host. The board system will work as a USB peripheral.

D: USB_DAT_SE0_U — Connect the USB controller to CON3, and connect USB cable from CON1 to USB host. The board system will work as a USB peripheral.

B: USB_DAT_SE0_B — Connect the USB controller to CON3, and connect USB cable from CON1 to USB host. The board system will work as a USB peripheral.

T: Audio Stereo — Go to Audio Stereo mode. Input an audio signal into the AUDIO_OUT port, you can hear the signal through headphone.

N: Audio Mono — Go to Audio Mono mode. Input an audio signal into the AUDIO_OUT port, and another audio signal into THE MIC_IN port. You can hear signals in the L and R speakers.

1: UART1 — Go to UART1 mode.

2: UART2 — Go to UART2 mode.

H: Hard Reset ISP1109 — Reset the ISP1109.

Esc: Exit to Main Menu — Return to the main menu.

6.2 ISA mode

6.2.1 Test mode

The port is connected to the ISA port of the development PC. To perform verification using test mode:

1. Switch off the development PC.

2. Remove all the unnecessary cards from the development PC.

3. Plug the ISP1109 ISA eval board into the ISA slot of the development PC.

4. Set JP1 to 1–OE and all switches and jumpers to their default states.

5. Switch on the development PC.

6. Run firmware 1109ISA.EXE on the development PC under DOS mode.

```
ISP1109 IC TEST FIRMWARE REV 1.20
Philips Electronics Singapore PTE. LTD. APIC
Getting more info on http://www.philips.com
or contact wired.support@philips.com
VenderID=0x04cc ProductID=0x1109  VersionID=0x0000
******************** ISP1109 Eva Main Menu ********************
                 Access register through
      S: SPI,                                    I: I2C,

                  User Mode select
      F: Functional mode,                    T: Test mode

Esc: Exit to Main Menu    Note: Green states are selected
******************** End  of  Main  Menu  ****************
Please select:
```

Fig 7.   Main menu

7. Select access mode as SPI or I^{2}C-bus by pressing the **S** or **I** key, respectively. Default is SPI.

8. Select user mode as test mode by pressing the **T** key.

```
******************** Test mode Menu  ********************
D: Data input             A: Address input
R: Read register          W: Write register
F: CLK SWITCH off         N: CLK SWITCH on
L: Interrupt en_low       U: Interrupt en_high
G: List all register

Esc : Exit to Main Menu    H: Hard Reset ISP1109
******************** End  of  Menu  ********************
Please select: _
```

Fig 8.   Test mode menu

9. Select the appropriate test action.

D: Data input — Input data to write to the register.

A: Address input — Input register address to write data to or read data from.

R: Read register — Read data from the Address register.

W: Write register — Write data to the Address register.

F: CLK SWITCH off — Switch off the ISP1109 internal clock.

N: CLK SWITCH on — Switch on the ISP1109 internal clock.

G: List all registers — Read and display all the registers.

L: Interrupt en_low — Set interrupt EN_LOW to verify whether the interrupt action is correct.

U: Interrupt en_high — Set interrupt EN_HIGH to verify whether the interrupt action is correct.

H: Hard Reset ISP1109 — Reset the ISP1109.

Esc: Exit to Main Menu — Return to the main menu.

6.2.2 Functional mode

The port is connected to the ISA port of the development PC. To perform verification using functional mode:

1. Switch off the development PC.
2. Remove all the unnecessary cards from the development PC.
3. Plug the ISP1109 ISA eval board into the ISA slot of the development PC.
4. Set JP3 and JP4 based on the selected states. Set JP1 to 1–OE and all other switches and jumpers to their default states. Plug audio source into the AUDIO_OUT port, headphones into the AUDIO_IN port, and microphone source into the MIC_IN port. Connect the USB controller to CON3.

- **USB mode**: Short JP3 1–2, JP4 1–2.
- **Audio mode**: Short JP3 3–4, JP4 3–4.
- **UART mode**: Short JP3 5–6, JP4 5–6, CON2 2–3.

5. Switch on the development PC.
6. Run firmware 1109ISA.EXE on the development PC under DOS mode.

Fig 9.   Main menu

7. Select access mode as SPI or I^{2}C-bus by pressing the **S** or **I** key, respectively. Default is SPI.
8. Select user mode as functional mode by pressing the **F** key.

Fig 10. Test menu

9. Select appropriate functional mode.

P: Pin — USB speed and suspend are controlled by the SPEED and SUSPEND pins.

R: Register — USB speed and suspend are controlled by the SPEED_REG and SUSPEND_REG register bits.

F: Full speed — Set USB speed to full-speed.

L: Low speed — Set USB speed to low-speed.

A: Active — Wake up from the suspend state.

S: Suspend — Go to the USB suspend state.

U: USB_VPVM_U — Connect the USB controller to CON3, and connect USB cable from CON1 to USB host. The board system will work as a USB peripheral.

V: USB_VPVM_B — Connect the USB controller to CON3, and connect USB cable from CON1 to USB host. The board system will work as a USB peripheral.

D: USB_DAT_SE0_U — Connect the USB controller to CON3, and connect USB cable from CON1 to USB host. The board system will work as a USB peripheral.

B: USB_DAT_SE0_B — Connect the USB controller to CON3, and connect USB cable from CON1 to USB host. The board system will work as a USB peripheral.

T: Audio Stereo — Go to Audio Stereo mode. Input audio signal into the AUDIO_OUT port, you can hear the signal through the headphone.

N: Audio Mono — Go to Audio Mono mode. Input an audio signal into the AUDIO_OUT port and another audio signal into the MIC_IN port. You can hear signals in the L and R speakers.

1: UART1 — Go to UART1 mode.

2: UART2 — Go to UART2 mode.

H: Hard Reset ISP1109 — Reset the ISP1109.

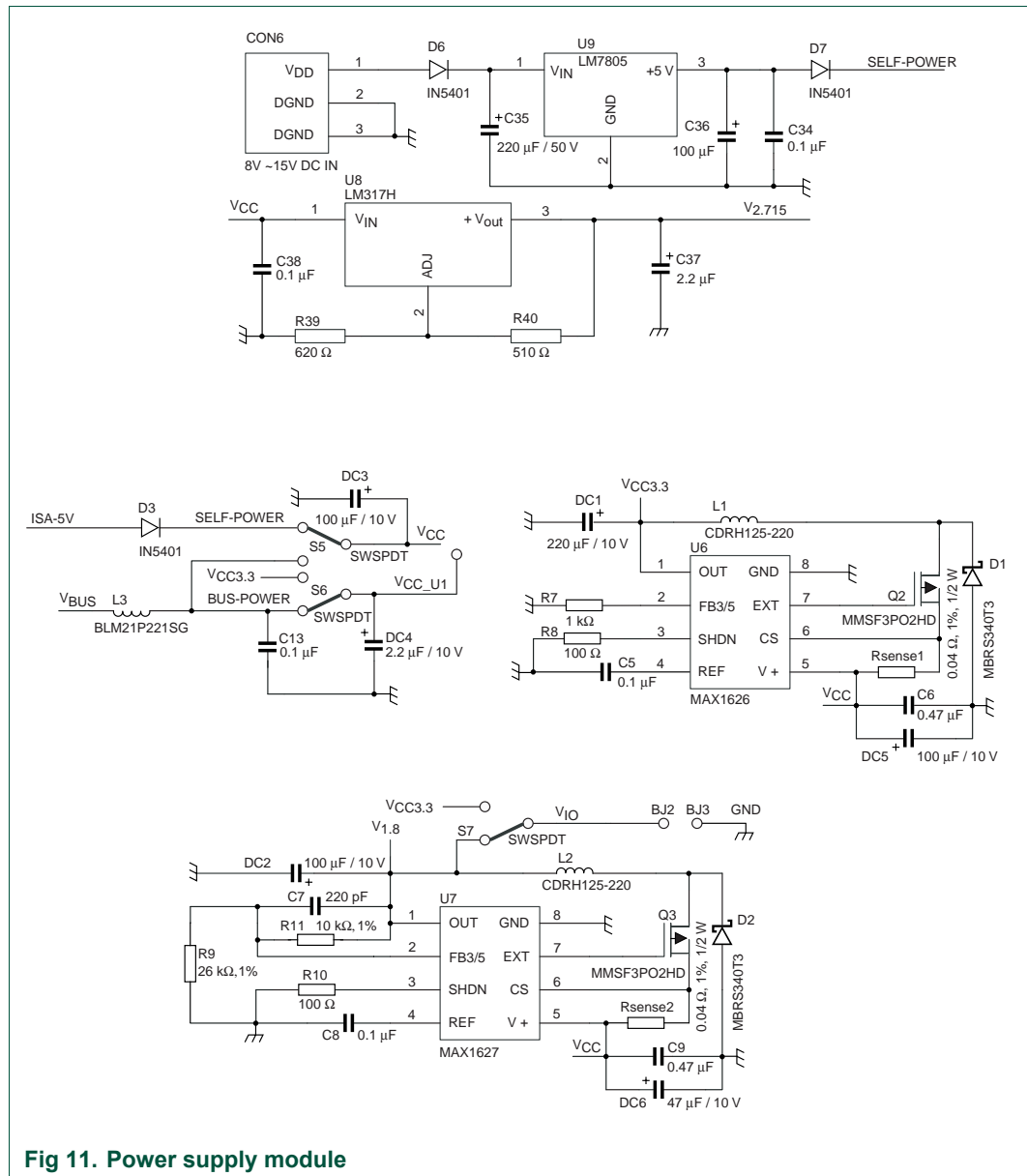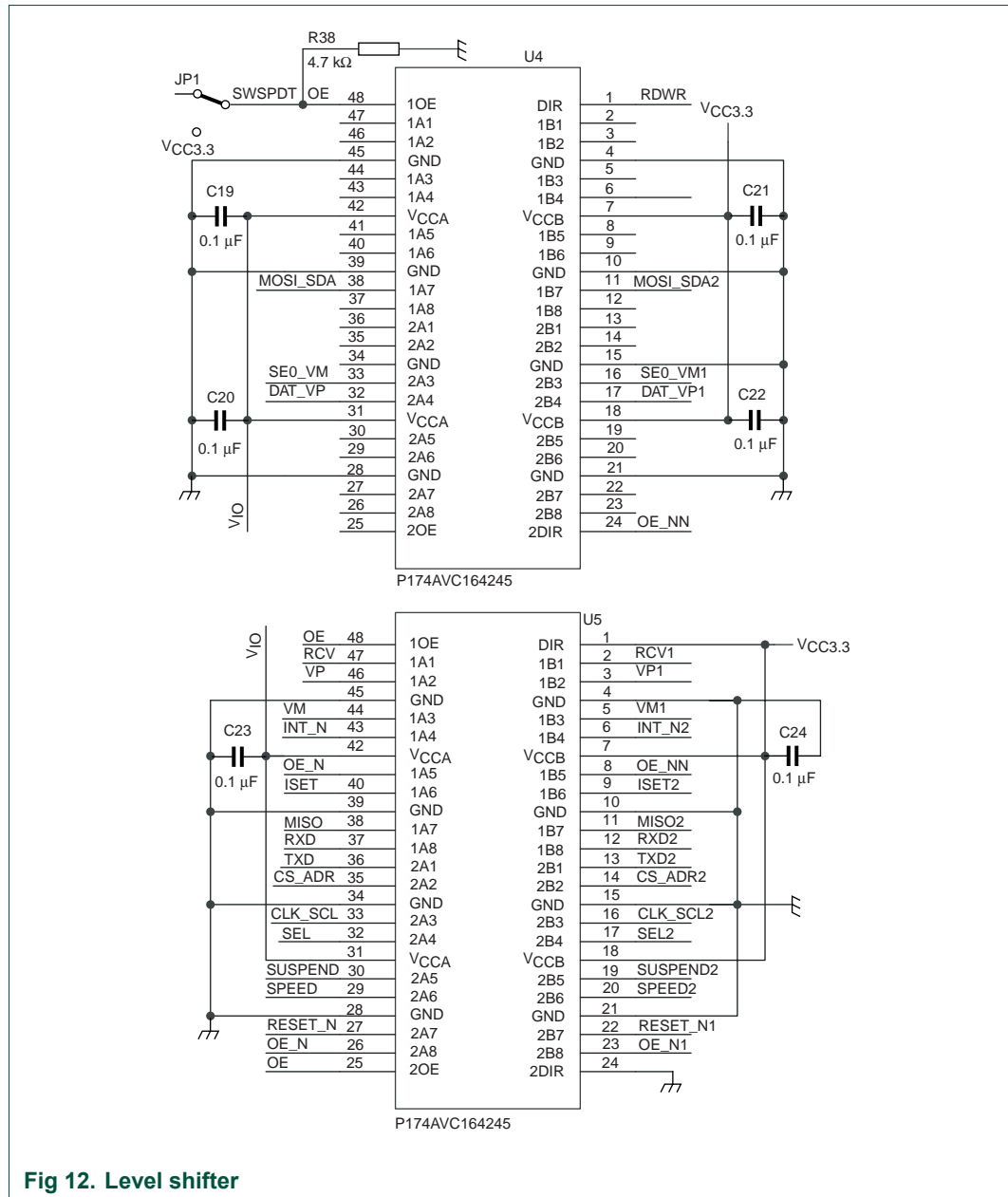**Esc: Exit to Main Menu —** Return to the main menu.
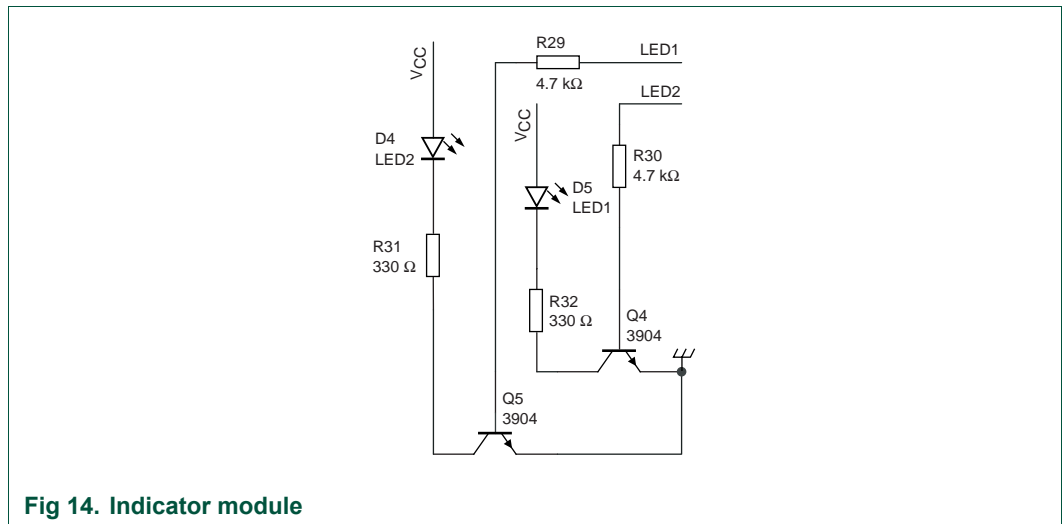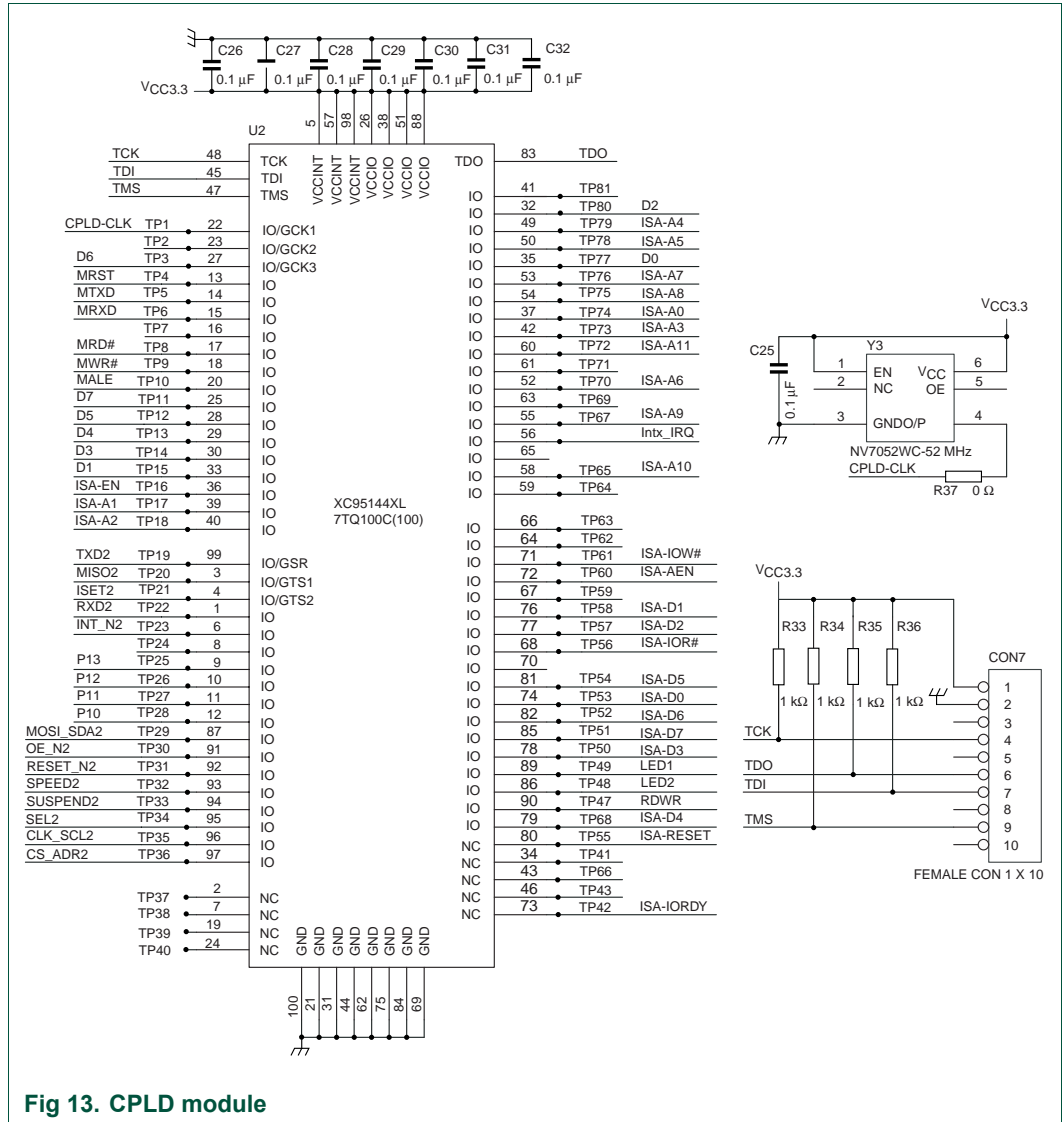
7. Schematics of the eval kit

Fig 11. Power supply module

Fig 12. Level shifter

Fig 13. CPLD module

Fig 14. Indicator module
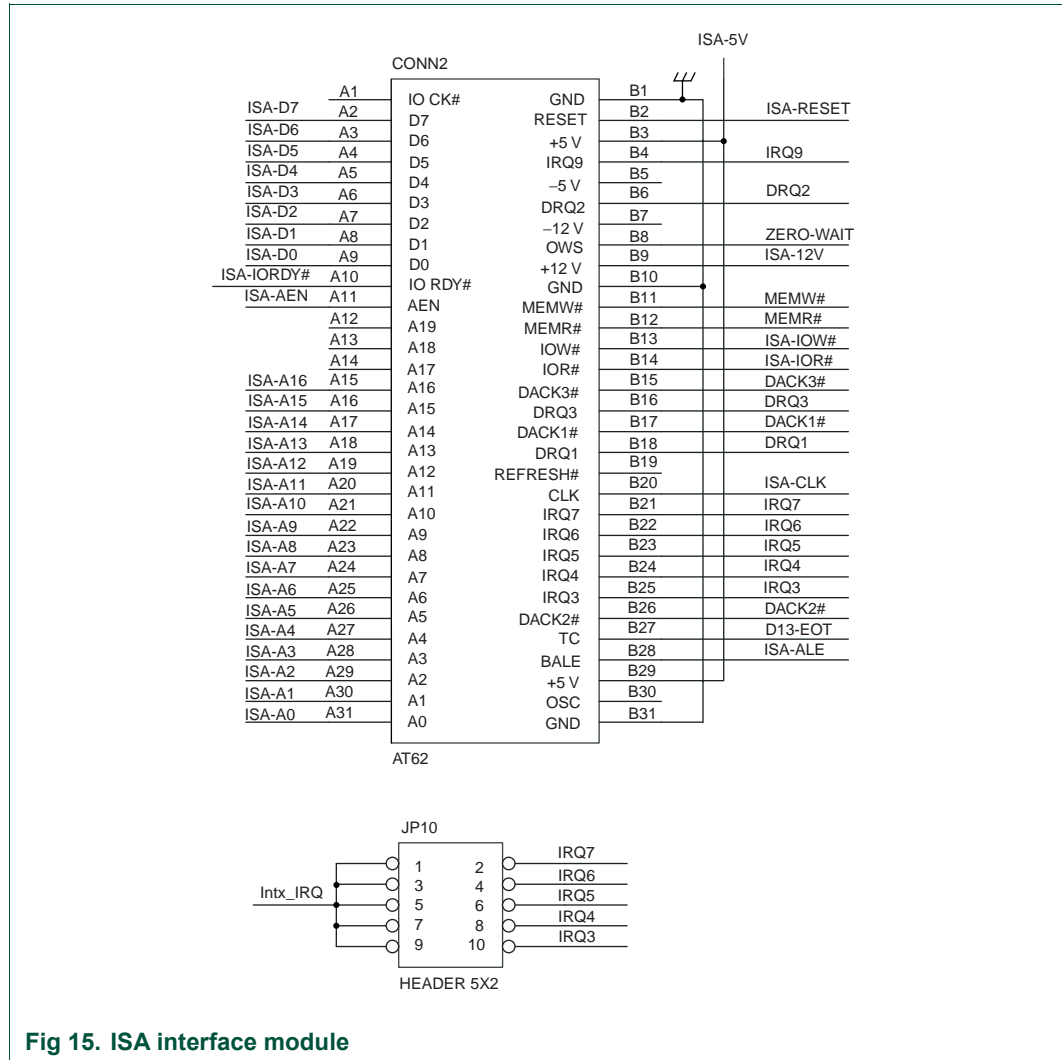
Fig 15. ISA interface module

Fig 16. Microprocessor module

Philips Semiconductors

UM10059

ISP1109 PC Eval Kit
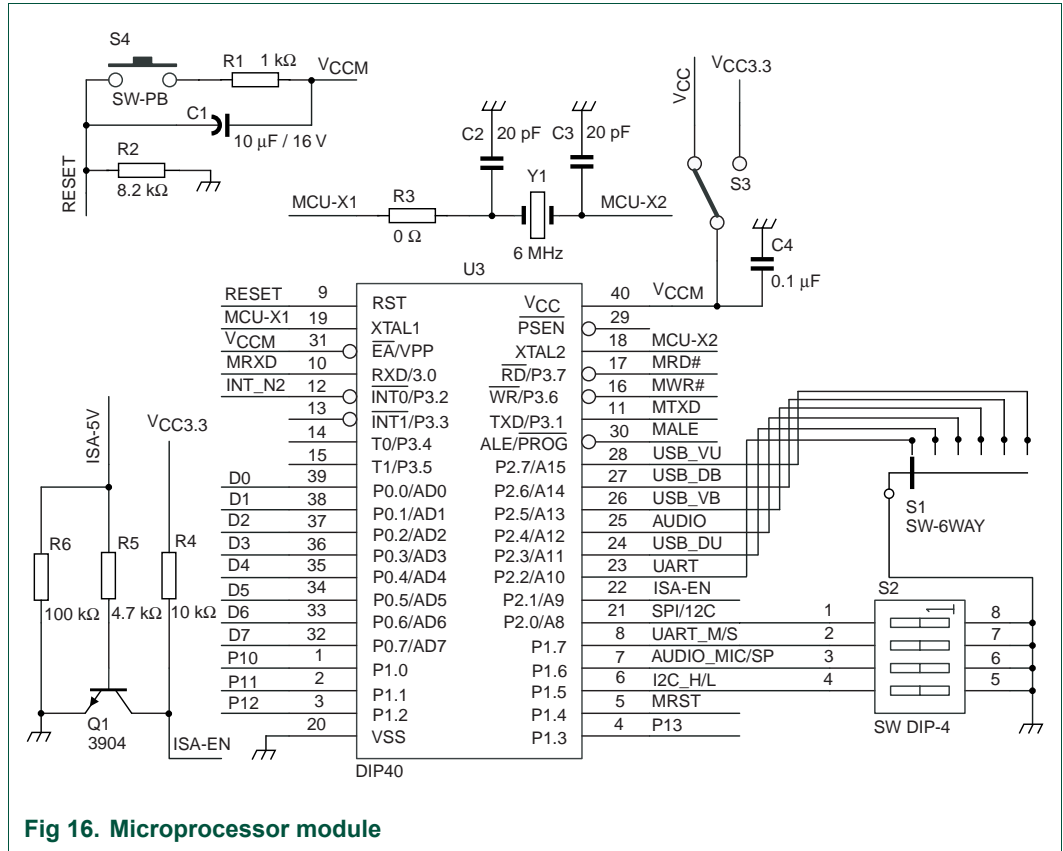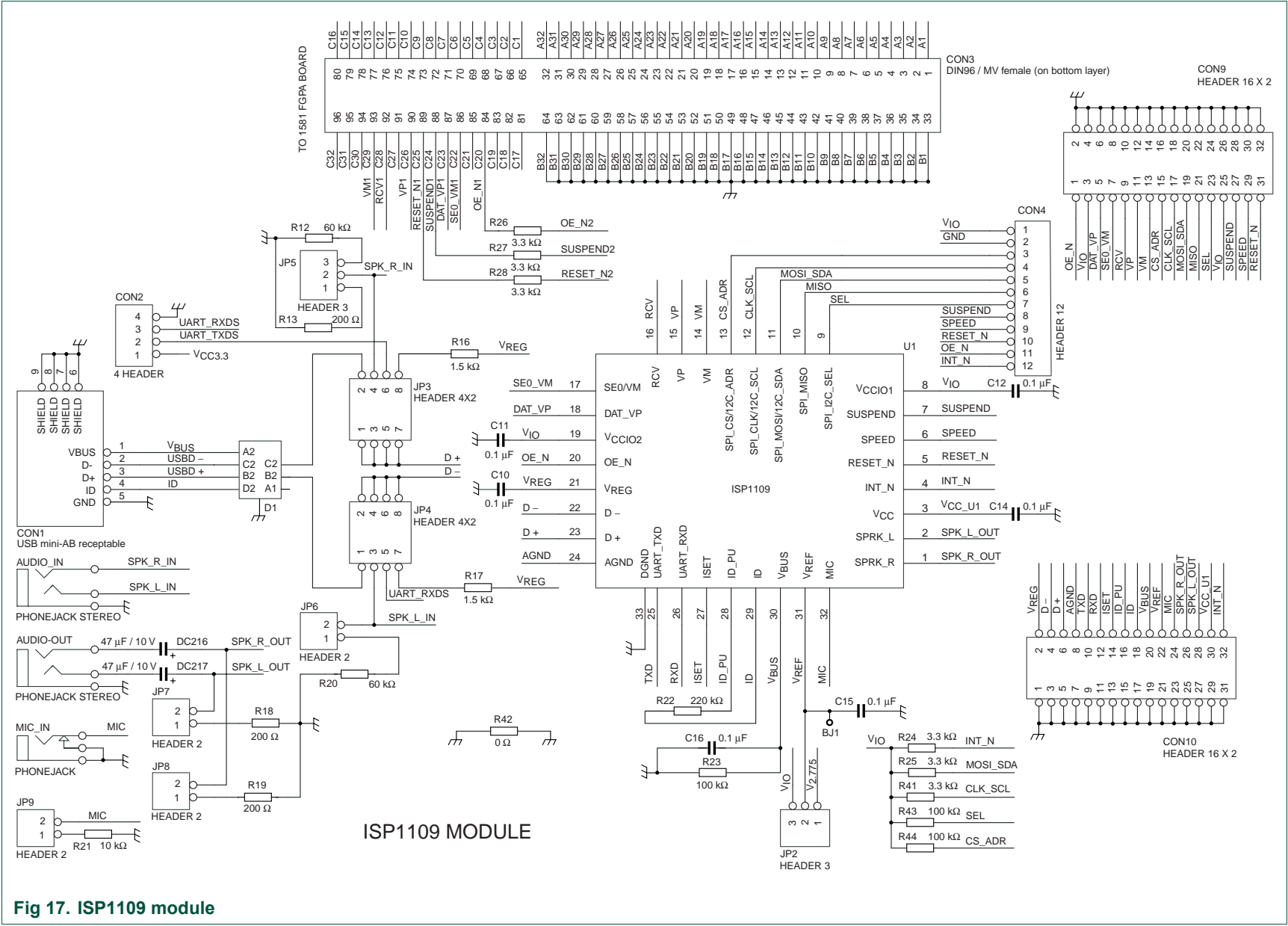
Fig 17. ISP1109 module

8. Bill of materials

Table 11: Bill of materials

Part type	Footprint	Designator
0 Ω	0805A	R42
0.04,1%, 1/2W	2010	Rsense1 Rsense2
0.1 µF	0805A	C13, C38, C5, C8, C14, C15, C16, C34, C25, C4, C10, C11, C12, C19, C20, C21, C22, C23, C24, C26, C27, C28, C29, C30, C31, C32
0.47 µF	0805A	C6, C9
0 Ω	0805A	R37, R3
1.5 kΩ	0805A	R17, R16
100 kΩ	0805A	R6 R44 R43 R23
100 Ω	0805A	R10 R8
100 µF	CASE D	C36
100 µF/10 V	CASE D	DC3 DC5 DC2
10 kΩ	0805A	R4 R21
10 kΩ, 1%	0805A	R11
10 µF/16 V	CASE D	C1
1 kΩ	0805A	R7 R36 R35 R1 R33 R34
2.2 µF	CASE A	C37
2.2 µF/10 V	CASE A	DC4
200 Ω	0805A	R13 R19 R18
20 pF	0805A	C2 C3
220 kΩ	0805A	R22
220 pF	0805A	C7
220 µF/10 V	CASE D	DC1
220 µF/50 V	CASE G	C35
22 pF	0805A	C17 C18
26 kΩ, 1%	0805A	R9
3.3 kΩ	0805A	R26 R27 R28
33 Ω	0805A	R14 R15
330 Ω	0805A	R31 R32
3904	3904A	Q1 Q4 Q5
3K3	0805A	R24 R41 R25
4 HEADER	HEADER 4	CON2
4.7 kΩ	0805A	R30 R29 R38
47 µF/10 V	CASE D	DC217 DC216 DC6

Part type	Footprint	Designator
4K7	0805A	R5
510 Ω	0805A	R40
60 kΩ	0805A	R12 R20
620 Ω	0805A	R39
6 MHz	HC49A	Y1
8~15 V DC IN	DCJACK	CON6
8K2	0805A	R2
AT62	ISA31GDA	CONN2
BANANA JACK	B JACK	BJ4 BJ3 BJ2 BJ1
BLM21P221SG	1206	L3
CDRH125-220	CDRH125	L1 L2
DIN96/MV FEMALE	DIN96-F	CON3
DIP40	DIP40A	U3
FEMALE CON 1 X 10	HD10A	CON7
HEADER 12	HEADER 12	CON4
HEADER 16 X 2	HEADER 16 X 2 - 2MM	CON10 CON9
HEADER 2	HEADER 2	JP9 JP8 JP7 JP6
HEADER 3	HEADER 3	JP2 JP5
HEADER 4 X 2	HEADER 4 X 2	JP3 JP4
HEADER 5 X 2	HD5 X 2A	JP10
IN5401	IN5401	D3 D6 D7
ISP1109	SOT617AA	U1
LED1	LED3MMA	D5
LED2	LED3MMA	D4
LM317H	TO-92	U8
LM7805	TO220	U9
MAX1626	SOIC8A	U6
MAX1627	SOIC8A	U7
MBRS340T3	MBRS340A	D1 D2
MMSF3PO2HD	MMSF3PO2HD	Q2 Q3
NV7052WC-52MHz	XTAL-SG8002	Y3
PHONEJACK	PHONEJACK	MIC_IN
PHONEJACK STEREO	PHONEJACK STEREO	AUDIO_OUT, AUDIO_IN
PI74AVC164245	TSSOP48A	U4 U5
SW DIP-4	SW DIP-4	S2

Part type	Footprint	Designator
SW SPDT	SW SPDT	S3 S7 S5 S6 JP1
SW-PB	PUSH-BTA	S4
SW-ROT	SW-ROT	S1
USB MINI-AB RECEPTACLE	USB MINI-AB	CON1
XC95144XL-7TQ100C (100)	TQFP100A	U2

9. References

- Universal Serial Bus Specification Rev. 2.0.
- ISP1109 Universal Serial Bus transceiver with carkit support data sheet
- CEA-936-A, Mini-USB Analog Carkit Interface.

10. Disclaimers

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